Please amend the subject application as follows:

IN THE CLAIMS:

/1.

(Original) A method for testing an integrated circuit, comprising:

providing a wafer having multiple die that are separated by a singulation area; providing a visual functional indicator for each of some or all of the multiple die; providing test circuitry for each of the some or all of the multiple die that have a visual functional indicator;

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for the some or all of the multiple die;

outputting a test result to the visual functional indicator for the some or all of the multiple die; and

using the test result to create a visual indication on the wafer with each visual functional indicator corresponding to the test result.

- 2. (Original) The method of claim 1 further comprising:

 physically locating the visual functional indicator within each of some or all of
 the multiple die.
 - 3. (Original) The method of claim 1 further comprising: physically locating the visual functional indicator external to the some or all of the multiple die and within a scribe area of the wafer.
- 4. (Original) The method of claim 1 further comprising:
 implementing the visual functional indicator as a light emitting diode (LED).
- J 5. (Original) The method of claim 1 further comprising:

 repeating the predetermined tests to test the some or all of the multiple die under a

 plurality of differing operating conditions to determine whether the some

multiple die.

or all of the multiple die are functional within a range of operating conditions.

- 6. (Original) The method of claim 1 further comprising:

 providing multiple visual indicators on each of the some or all of the die, each of
 the multiple visual indicators indicating functional operation of a separate
 predetermined portion of a predetermined one of the some or all of the
- (Original) The method of claim 1 further comprising:

 implementing the visual functional indicator as a binary coded decimal (BCD)

 light emitting diode (LED) that asserts a predetermined decimal upon
 passing a corresponding predetermined functional test.
- 8. (Original) The method of claim 1 further comprising:
 singulating the multiple die and segregating functional die of the multiple die
 from non-functional die of the multiple die based upon the visual
 indication.
- (Original) The method of claim 1 further comprising:

 recording the visual indication with either a camera or a high resolution imager to

 form a data base that is used by a singulation tool to singulate the multiple

 die and segregate the multiple die based on the visual indication.

Cancel claims 10-19.

20. (Newly Presented) A method for testing an integrated circuit, comprising:

providing a wafer having multiple die that are separated by a singulation area;

providing a visual functional indicator for each of the multiple die thereby

providing a plurality of visual indicators;

providing test circuitry for each of the multiple die;

die: and --

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for each of the multiple die; outputting a test result to the visual functional indicator for each of the multiple

using the test result to create a visual indication on the wafer with each visual functional indicator corresponding to the test result.

- 21. (Newly Presented) The method of claim 20 further comprising:
 using a portion of the plurality of visual indicators for both a test mode of
 operation and a normal functional mode of operation.
- 22. (Newly Presented) The method of claim 20 further comprising:

 positioning each respective visual functional indicator within a corresponding respective one of the multiple die.
- 23. (Newly Presented) The method of claim 20 further comprising: implementing each visual functional indicator with a light emitting diode (LED).
- 24. (Newly Presented) A method for testing an integrated circuit, comprising:

 providing a wafer having multiple die;

 providing a visual functional indicator for each of the multiple die;

 providing test circuitry for each of the multiple die that have a visual functional indicator;

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for the multiple die; and outputting a test result to each visual functional indicator to visually indicate which die of the multiple die passed the predetermined tests and which die failed the predetermined tests.

Onto

(Newly Presented) The method of claim 24 further comprising:

physically locating each functional indicator within a scribe area of the wafer.

(Newly Presented) The method of claim 24 further comprising:

recording each visual functional indicator with either a camera or a high

resolution imager to form a data base that is used by a singulation

tool to singulate the multiple die and segregate the multiple die

based on each visual functional indicator.